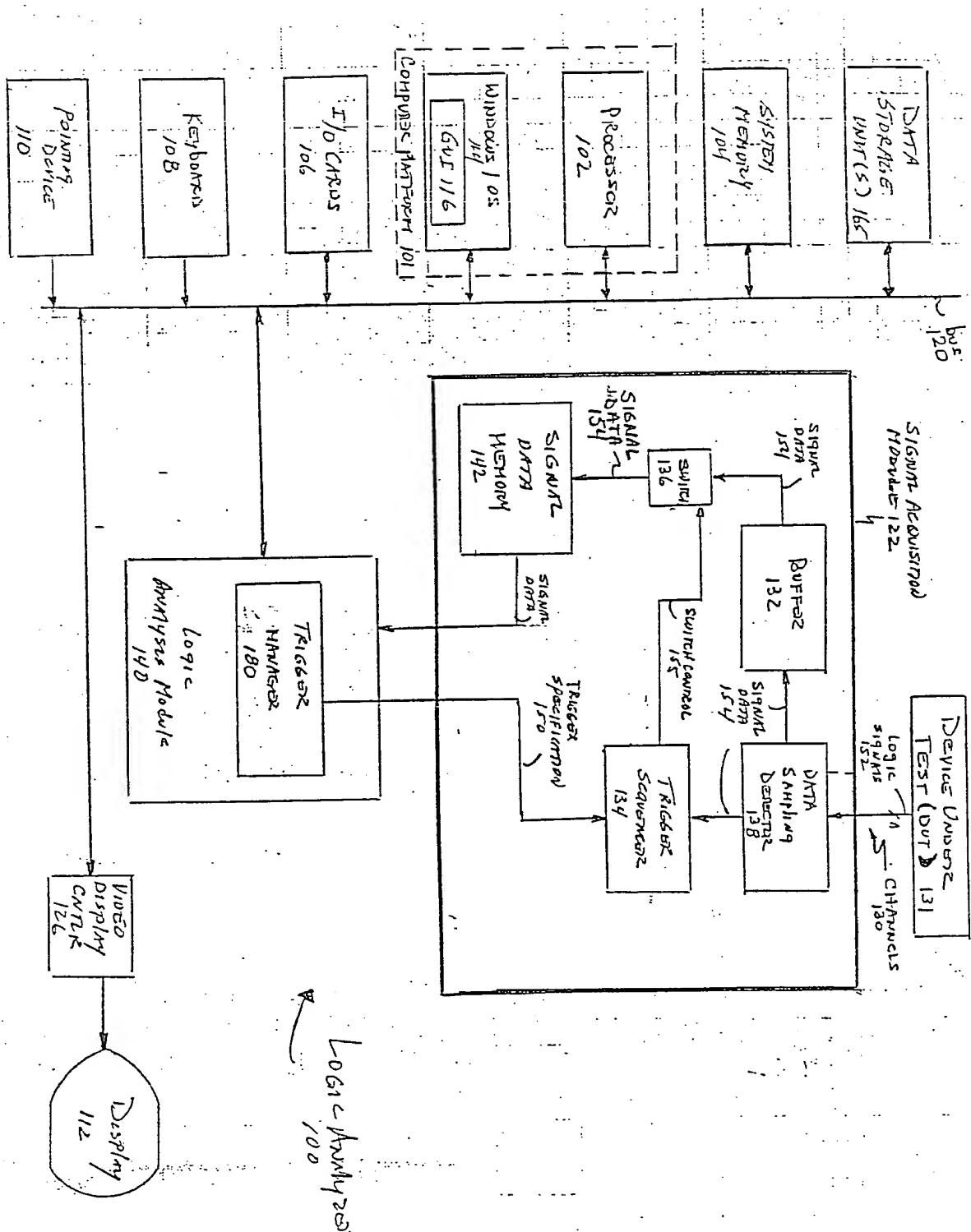


FIG 1



03616278 071400

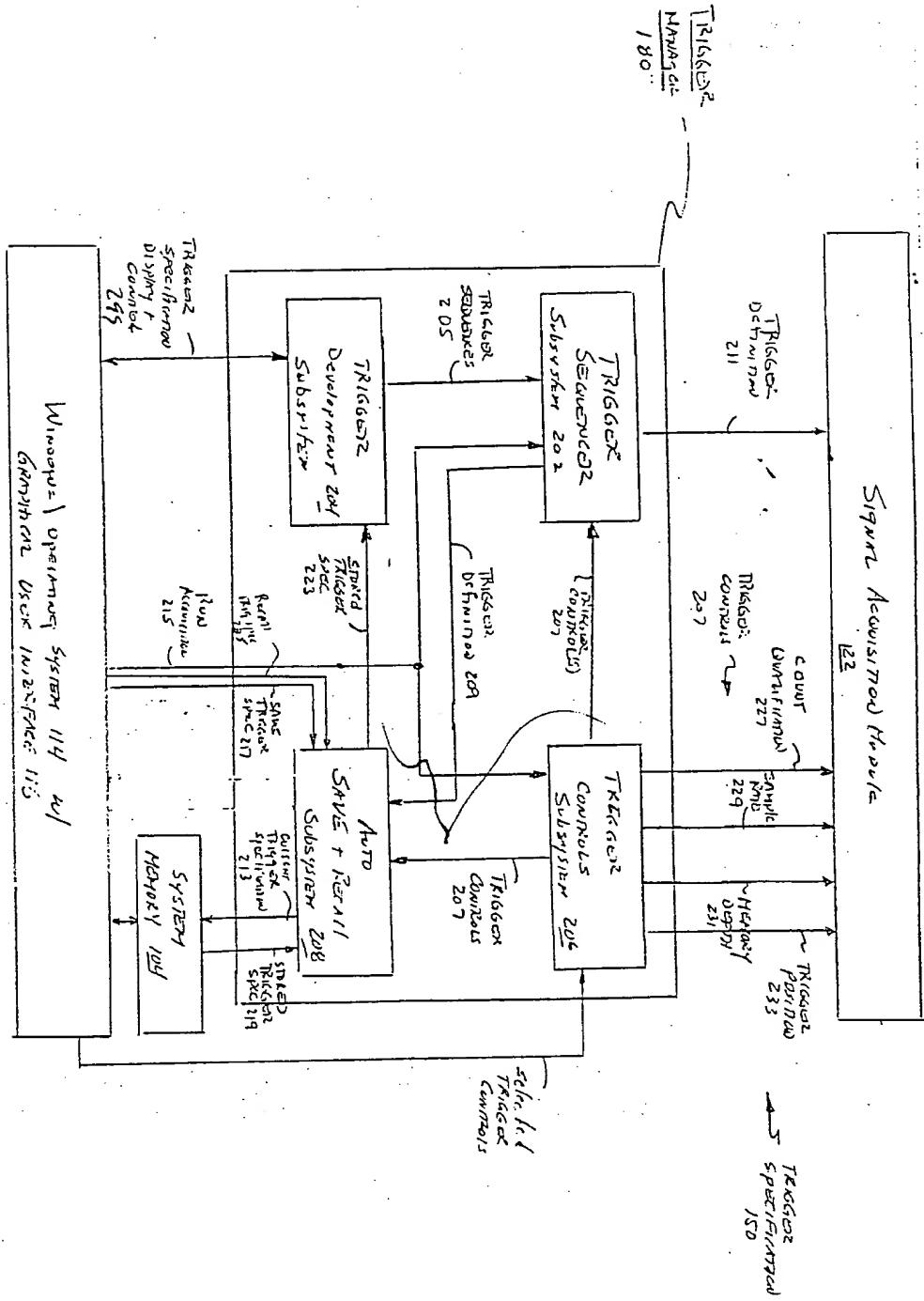
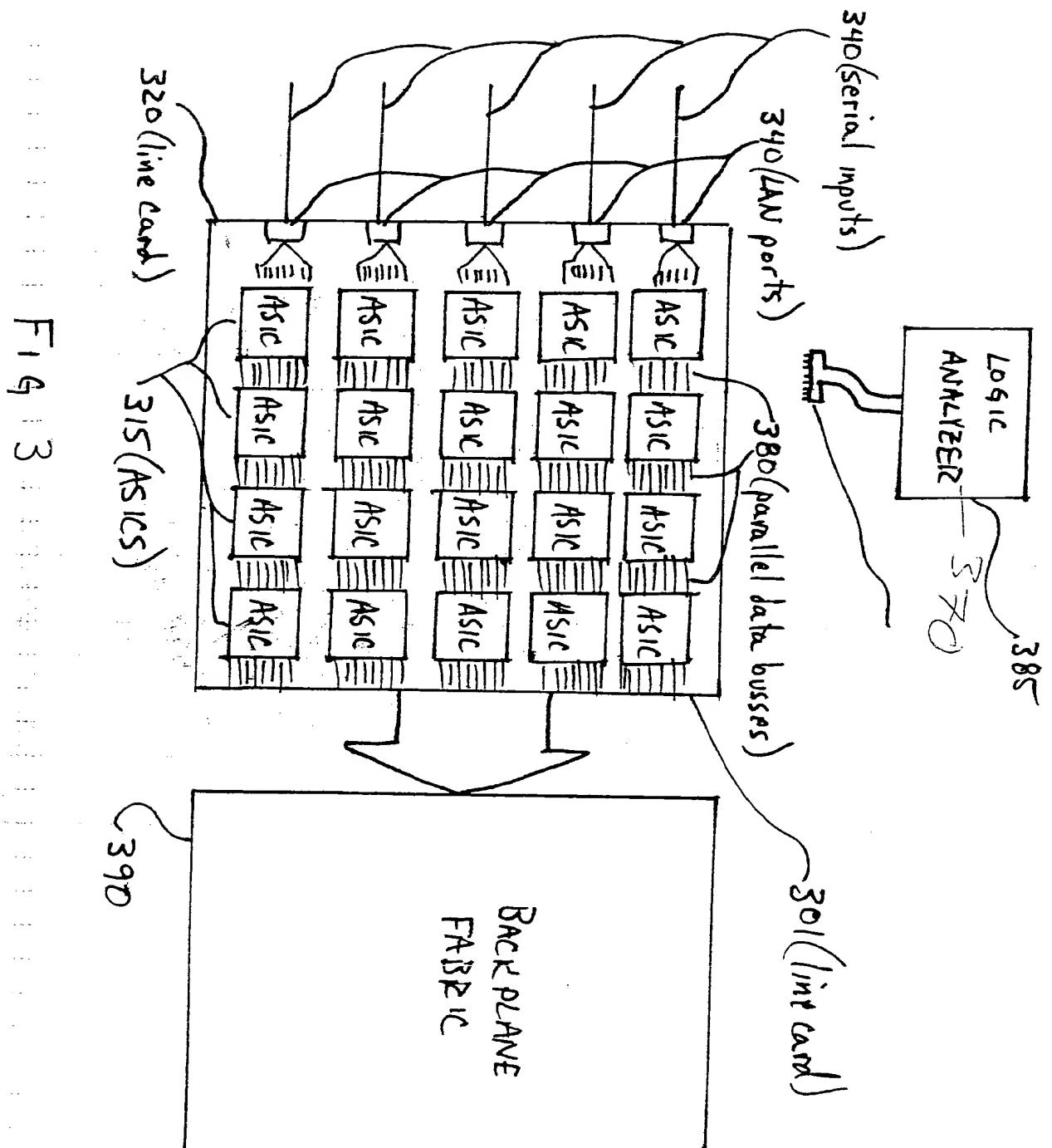


Figure 2



09616273 - 071400

FIG 13

Destination Address:	48 bits:	1 1-XX-XX-1 1-XX-XX-XX
Source Address:	48 bits:	XX-XX-XX-XX-XX-XX-XX
Length/type:	16 bits:	XXXX

Fig. 4a

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Fig. 4b

Destination Address: 48 bits: XX-XX-XX-1 1-XX-XX-XX
Source Address: 48 bits: XX-XX-XX-XX-XX-XX-XX-XX
Length/type: 16 bits: 0800

Fig. 4c

<u>Data Bit Block</u>	<u>Don't Care Mask</u>
11	00
00	ff
00	ff
11	00
00	ff
08	00
00	00

Fig. 4d

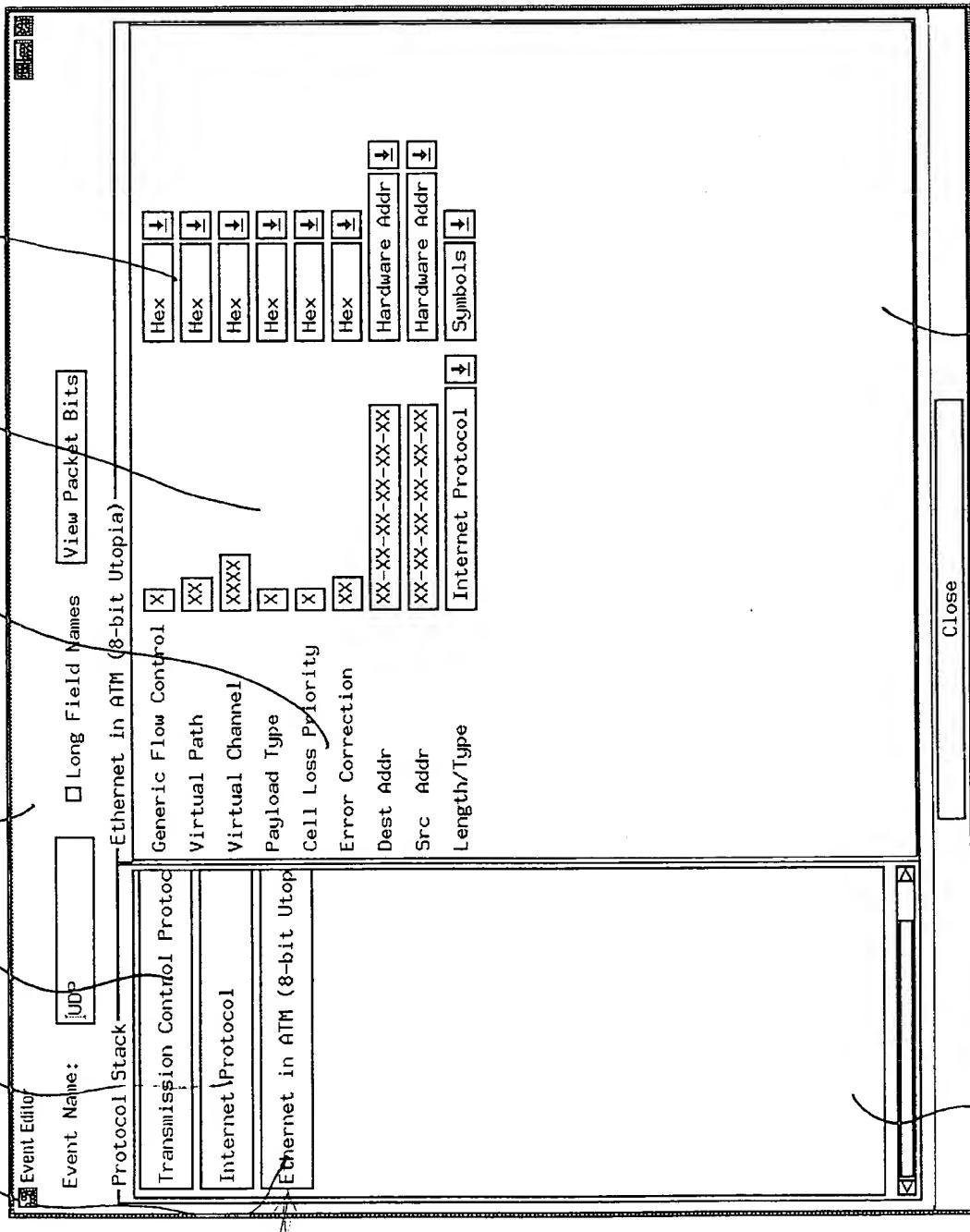


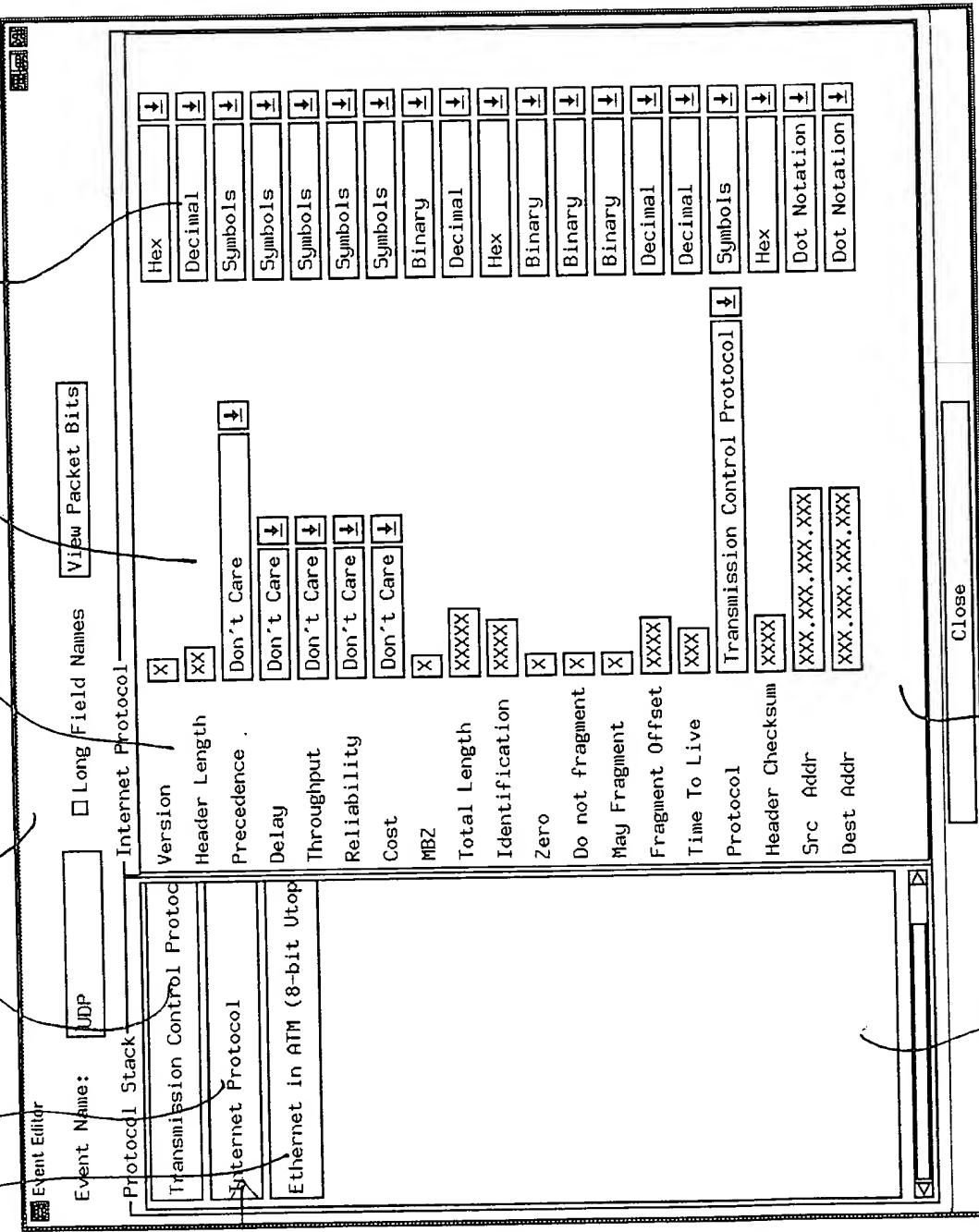
Fig 5

521 522 523
524 525 526 527 528 529

530

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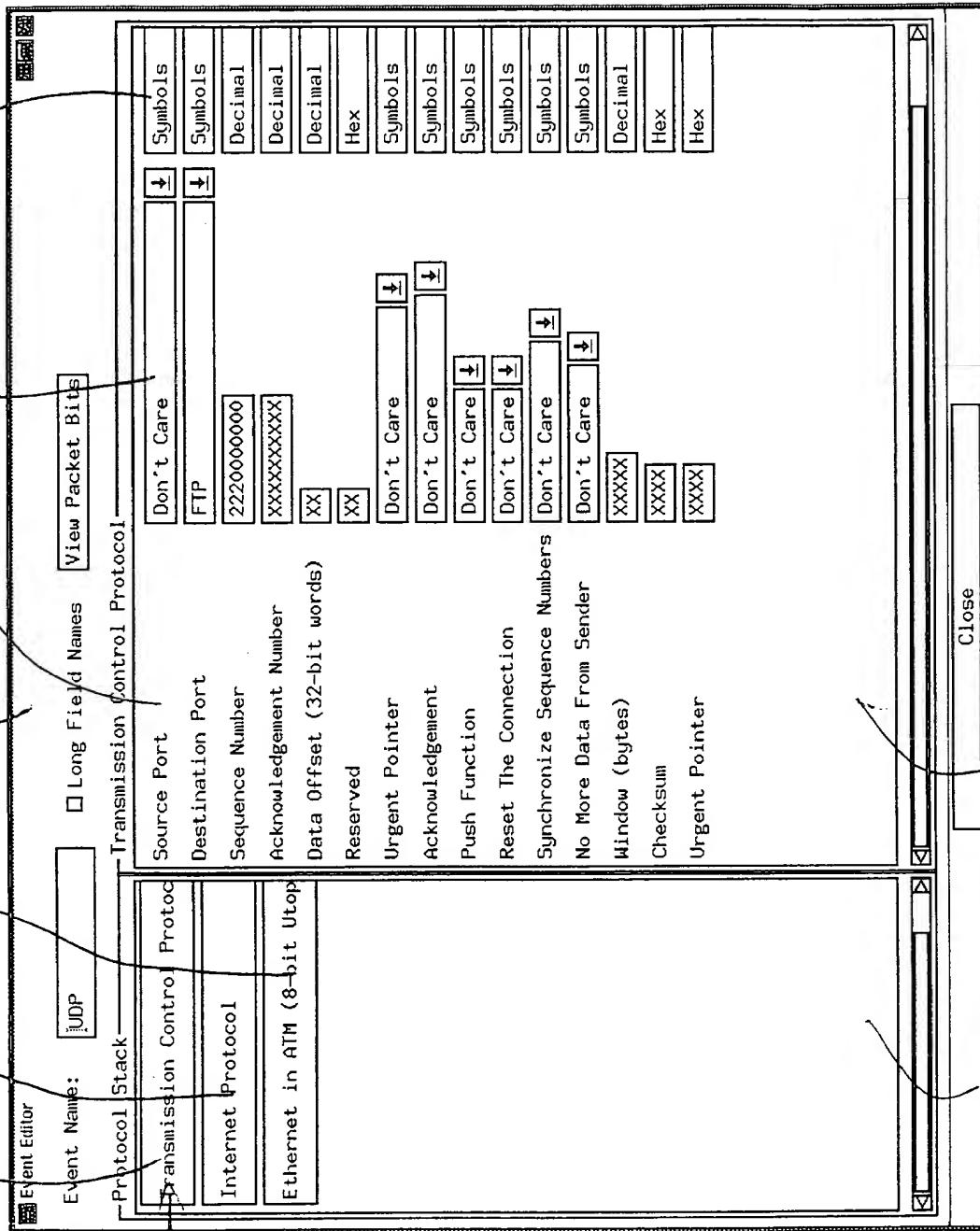
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Fig 6

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Analyzer-D2 - 333MHz State/2GHz Timing Zoom 2M San - x

File Window Edit Options Clear Help

Sampling | **Format** | **Trigger** | **Symbol** | **Sequence**

805

Event #1 - Packet E X

801	0.....8....15
802	0XXXXXXXXXXXXX
803	1XXXXXXXXXXXXX
804	2XXXXXXXXXXXXX
805	3XXXXXXXXXXXXX
806	4XXXXXXXXXXXXX
807	5XXXXXXXXXXXXX
808	6000100000000000
809	7XXXXXXXXXXXXX
810	8XXXXXXXXXXXXX
811	9XXXXXXXXXXXXX
812	10XXXXXXXXXXXX
813	11XXXXXXXXXXXX000001
814	12XXXXXXXXXXXXXX
815	1300001011000001011
816	1400001011000001011
817	1500001011000001011
818	1600001011000001011
819	17XXXXXXXXXXXXXX
820	18XXXXXXXXXXXXXX

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FIG 8

13-16